In the Claims

1. A method of identifying faulty programmable interconnect resources of a field programmable gate array during normal on-line operation comprising the steps of:

configuring said field programmable gate array into a self-testing area and a working area, said working area maintaining normal operation of the field programmable gate array;

testing programmable interconnect resources located within said self-testing area for faults;

identifying at least one programmable interconnect resource having a fault detected during said testing step.

2. The method set forth in Claim 1, wherein the step of testing said programmable interconnect resources located within said initial self-testing area for faults includes propagating test patterns along at least two groups of wires under test;

comparing outputs of said at least two groups of wires under test; and

producing fault status data for said at least two groups of wires under test.

3. The method of identifying faulty programmable interconnect resources set forth in claim 2, wherein said identifying step includes minimizing a region of one of said groups of wires under test which includes said fault.

4. The method of identifying faulty programmable interconnect resources set forth in claim 3, wherein said identifying step includes reconfiguring said minimized region of said group of wires under test for further testing in order to identify a wire within said minimized region which includes said fault.

5. The method of identifying faulty programmable interconnect resources set forth in claim 4, wherein said identifying step includes replacing programmable interconnect resources within said wire for further testing in order to identify a wire segment, a configuration interconnect point, and/or a combination thereof which includes said fault.

6. The method of identifying faulty programmable interconnect resources set forth in claim 2, wherein said identifying step includes reconfiguring said groups of wires under test for further testing in order to identify a wire within said groups of wires under test which includes said fault.

7. The method of identifying faulty programmable interconnect resources set forth in claim 6, wherein said identifying step includes minimizing a region of said wire which includes said fault.

8. The method of identifying faulty programmable interconnect resources set forth in claim 7, wherein said identifying step includes replacing programmable interconnect resources within said minimized region of said wire for further testing in order to identify a wire segment, a configuration interconnect point, and/or a combination thereof which includes said fault.

9. A method of identifying faulty programmable interconnect resources of a field programmable gate array during normal on-line operation comprising the steps of:

configuring said field programmable gate array into a self-testing area and a working area, said working area maintaining normal operation of the field programmable gate array;

testing groups of programmable interconnect resources located within said self-testing area for faulty resources;

minimizing a region of at least one of said groups of programmable interconnect resources determined to include said faulty resource;

reconfiguring said region for further testing in order to identify said faulty resource detected during said initial testing step; and

repeating the steps of reconfiguring and testing until said faulty resource is identified.

10. The method of identifying faulty programmable interconnect resources set forth in claim 9, wherein said self-testing area includes programmable logic blocks configured to function as at least one test pattern generator and at least one output response analyzer, and programmable interconnect resources configured as at least two groups of wires under test.

11. The method of identifying faulty programmable interconnect resources set forth in claim 10, wherein the step of testing said groups of programmable interconnect resources includes propagating test patterns generated by said at least one test pattern generator along said at least two groups of wires under test, comparing outputs of said at least two groups of wires under test using said at least one output response analyzer, and producing fault status data for said at least two groups of wires under test.

12. The method of identifying faulty programmable interconnect resources set forth in claim 11, wherein the step of testing said groups of programmable interconnect resources includes comparing the outputs of said at least two groups of wires under test with an output of at least one additional group of wires under test in order to determine which of said at least two groups of wires under test includes said faulty resource

detected during said initial testing step.

13. The method of identifying faulty programmable interconnect resources set forth in claim 12, wherein the step of minimizing a region of said at least one group of programmable interconnect resources determined to include said faulty resource includes establishing said interconnect resources located within said self-testing area as at least two subsequent groups of wires under test, at least one of said subsequent groups including a subdivided portion of said resources located within said faulty group of wires under test; and

testing resources located within said subsequent groups of wires under test for faults in order to determine which subsequent group of wires under test includes said faulty resource.

14. The method of identifying faulty programmable interconnect resources set forth in claim 13, wherein the steps of establishing and testing are repeated until the region of said group of wires under test which includes said faulty resource is minimized.

15. The method of identifying faulty programmable interconnect resources set forth in claim 14, wherein the step of reconfiguring said region includes re-routing programmable interconnect resources within said minimized region to avoid suspect resources for further testing in order to identify a wire segment, a configuration interconnect point, and/or a combination thereof which includes said fault.

16. The method of identifying faulty programmable interconnect resources set forth in claim 9, further comprising the step of roving said self-testing area by reconfiguring the field programmable gate array such that a portion of the working area becomes a subsequent self-testing area and at least a portion of the initial self-testing area becomes a portion of the working area.

17. An apparatus for identifying faulty programmable interconnect resources of a field programmable gate array comprising:

a controller in communication with the field programmable gate array for: (a) configuring the field programmable gate array into a self-testing area and a working area, the working area maintaining normal operation of the field programmable gate array; (b) initiating testing of groups of programmable interconnect resources located within the self-testing area for faults; (c) reconfiguring groups of resources determined to include a faulty resource for further testing in order to minimize a region of the group of resources which includes the faulty resource; (d) repeating the steps of testing and reconfiguring until the region of the group of resources which include the faulty resource is minimized; (e) reconfiguring the resources located within the minimized faulty region of the group of resources for further testing in order to identify the faulty resource by re-routing portions of the minimized faulty region to avoid suspect resources; and (f) repeating the steps of reconfiguring and further testing until the faulty resource is identified.

18. The apparatus for identifying faulty programmable

interconnect resources of a field programmable gate array of claim 17, further comprising a storage medium in communication with said controller for storing a functional configuration of the field programmable gate array, a plurality of test configurations, and fault status data.

19. The apparatus for identifying faulty programmable interconnect resources of a field programmable gate array of claim 18, wherein said self-testing area includes programmable logic blocks configured to function as at least one test pattern generator and at least one output response analyzer, and programmable interconnect resources configured as at least two groups of wires under test; and

wherein test patterns generated by said at least one test pattern generator are propagated along said at least two groups of wires under test, outputs of said at least two groups of wires under test are compared using said at least one output response analyzer, and fault status data for said at least two groups of wires under test is produced.

20. The apparatus for identifying faulty programmable interconnect resources of a field programmable gate array of claim 17, wherein said self-testing area roves by reconfiguring the field programmable gate array such that a portion of the working area becomes a subsequent self-testing area and at least a portion of the initial self-testing area becomes a portion of the working area.

21. A method of identifying faulty programmable interconnect resources of a field programmable gate array comprising the steps of:

configuring programmable logic blocks of said field programmable gate array to function as at least one test pattern generator and at least one output response analyzer, and programmable interconnect resources as at least two groups of wires under test;

testing said at least two groups of wires under test faults;

identifying at least one programmable interconnect resource having a fault detected during said testing step.

22. The method of identifying faulty programmable interconnect resources set forth in claim 21, wherein the step of testing said at least two groups of wires under test for faults includes propagating test patterns along said least two groups of wires under test;

comparing outputs of said at least two groups of wires under test; and

producing fault status data for said at least two groups of wires under test.

23. The method of identifying faulty programmable interconnect resources set forth in claim 22, wherein said identifying step includes minimizing a region of one of said groups of wires under test which includes said fault.

24. The method of identifying faulty programmable interconnect resources set forth in claim 23, wherein said identifying step includes reconfiguring said minimized region of said group of wires under test for further testing in order to identify a wire within said minimized region

which includes said fault.

25. The method of identifying faulty programmable interconnect resources set forth in claim 24, wherein said identifying step includes replacing programmable interconnect resources within said wire for further testing in order to identify a wire segment, a configuration interconnect point, and/or a combination thereof which includes said fault.

26. The method of identifying faulty programmable interconnect resources set forth in claim 22, wherein said identifying step includes reconfiguring said groups of wires under test for further testing in order to identify a wire within said groups of wires under test which includes said fault.

27. The method of identifying faulty programmable interconnect resources set forth in claim 26, wherein said identifying step includes minimizing a region of said wire which includes said fault.

28. The method of identifying faulty programmable interconnect resources set forth in claim 27, wherein said identifying step includes replacing programmable interconnect resources within said minimized region of said wire for further testing in order to identify a wire segment, a configuration interconnect point, and/or a combination thereof which includes said fault.